eWLCSP

Encapsulated Wafer Level Chip Scale Package

A compelling value proposition over standard WLCSP, this innovative encapsulated WLCSP technology offers the combined benefits of superior quality, lower cost structure and ease of conversion through drop-in replacement.

Highlights

- Innovative FlexLine™ manufacturing approach delivers compelling cost reductions over standard WLCSP
- Seamless conversion between fan-in and fan-out designs with the same basic package platform
- Unique WLP manufacturing approach independent of incoming silicon wafer diameter

Features

Process

- Wafer agnostic process normalises wafer diameter to uniform processing size making incoming wafer size irrelevant
- All processing performed in wafer form before dicing
- eWLCSP structure identical to conventional WLCSP with exception of protective sidewall coating
- Final back grind thins the package to desired thickness
- Backside surface can be covered with mold compound, exposed with grind process or laminated with protective film
- Standard photolithography; Plated Cu RDL, Plated Cu UBM
- At least 30µm routing space at package edge compared to Si WLCSP
- Typical body thickness: ~300µm
- Same body sizes available as WLCSP (qualified up to 6x6mm); eWLCSP die size can be scaled beyond 6x6mm
- Ball pitch 0.50mm, 0.40mm, 0.35mm
- Fan-out panel/wafer level test before dicing
- Package singulation without touching Si after testing

Quality

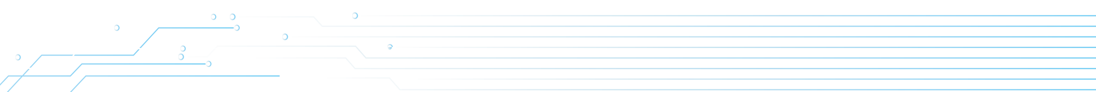
- Polymer sidewall offers mechanical protection from die chipping, cracking and other handling issues
- >50% increase in die strength over traditional WLCSP structures
- Advanced dielectrics provide equal/better reliability and performance
- Benefits optimal for larger WLCSP die sizes
- Passes standard CLR, BLR, temperature cycle on board (TCoB) and drop test (equivalent to WLCSP)

Cost

- Drop-in replacement offers low risk, seamless conversion path from standard WLCSP
- Increased savings as panel sizes increase
- FlexLine process qualified at advanced silicon nodes down to 22/20nm

Robust Fan-in WLP Solution

Customers with robust reliability requirements have the option of encapsulating the back and four sidewalls of a WLCSP die. This provides mechanical robustness and resistance to chipping, cracking and handling damage, enabling improved long term reliability over traditional bare die WLCSP. Encapsulation also provides significant



Process Highlights

Passivation	1 via size: 20µm (minimum)
RL Line/Space	8µm line/8µm space (minimum)
Bump Pitch	0.50mm, 0.4mm, 0.35mm, 0.3mm
Visual Inspection	Automatic optical inspection with electronic wafer mapping

Test Services

Wafer level testing is an important process for yield enhancement and a final test requirement for eWLCSP. Our best-in-class test services include:

- Product Engineering support
- Probe capability
- Program generation/conversion
- High volume wafer sort

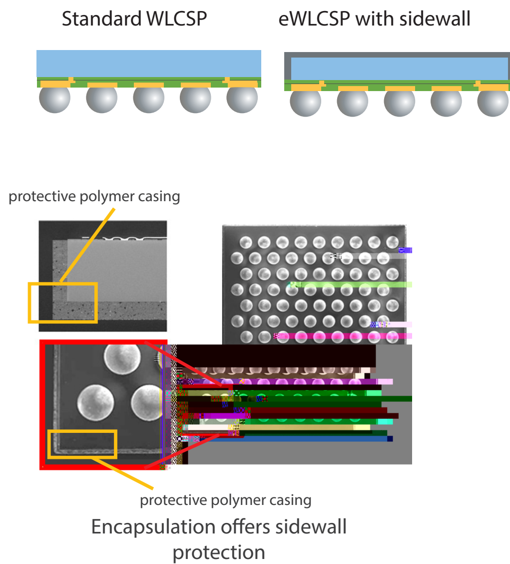
Applications

eWLCSP is a compelling solution for space constrained mobile devices and new applications such as wearable technology and automotive markets. Effective transition to eWLCSP is optimal for the following applications:

- 200mm WLCSP migration to FlexLine for PMIC and MCU applications
- 300mm WLCSP migration to eWLCSP for amplifiers, MCU, PMIC and RFIC applications

Cross Sections

(Not to scale)



Encapsulation offers sidewall protection

Component Level Reliability Testing

Moisture Sensitivity Level	MSL1, (260°C, 3x)
Temperature Cycling after Precon	-55°C/125°C, 1000 cycles
Unbiased HAST after Precon	130°C/85% RH, 192 hrs
High Temperature Storage	150°C, 1000 hrs
Temperature Humidity Bias Test	85°C/85%/5V, 1000 hrs
Ball Shear Test	Post reflow: T0, 5X and 10X; reflow: 260 +0/-5 °C

Thermal Performance

- Thermal performance in the 20-40°C/W range for a 5mm x 5mm die without thermal enhancement
- Application specific thermal characterization available upon request

Electrical Performance

- Dependent on application design, and capable to beyond 10GHz
- Application specific electrical characterization available upon request
- Thick Cu for high current low inductance applications