PBGA-MD

Plastic Ball Grid Array - Multi-Die

Highlights

- Strip molded, cost-effective, high I/O, multi-die packaging solution
- Enables space efficient side by side and stacked die packaging options
- Wide range of pre-existing body sizes
- Available in eutectic and Pb-free bill of materials

Features

- Full in-house package and substrate design capability
- Full in-house electrical, thermal and mechanical simulation and measurement capability
- Multiple metal layer options for signal, power and ground planes for improved electrical performance
- Flexible body sizes ranging from 15mm x 15mm to 40mm x 40mm
- Accommodates both side by side and/or stacked die configurations
- Multiple chip design and optional passive / discrete components available (SiP)
- 0.65, 0.80, 1.00, 1.27mm and 1.5mm ball pitch with greater than 1000 I/O available
- Perimeter or full ball array
- SnPb and Pb-free balls available
- Pb-free and green material set options
- JEDEC standard compliant

Description

BGA packages can be used for high performance applications with high I/O connections and high thermal and electrical requirements. The characteristics of BGA packages make them suitable for a wide variety of devices used in computing platforms, networking, hand-held consumer products, wireless communications devices, video cameras, home electronic devices and game consoles.

Plastic Ball Grid Array - Multi-Die (PBGA-MD) packages utilize laminate substrates and are available in a variety of standard JEDEC body sizes

Specifications

Die Thickness	150-381μm (6-15mils)
Gold Wire	15-30μm (0.6/0.7/0.8/0.9/1.0/1.1/1.2mils) diameter
Pd/Cu Wire	15-30μm (0.6/0.7/0.8/1.0mils) diameter
Bond Pad Pitch	45μm inline or 25/50μm staggered capable
Mold Cap Thickness	0.7-1.17mm
Marking	Laser
Packing Options	JEDEC tray/tape & reel

Reliability

Moisture Sensitivity Level	JEDEC Level 3
Temperature Cycling	–65°C/150°C, 1000 cycles (typical)
High Temperature Storage	150°C, 1000 hrs (typical)
Pressure Cooker Test	121°C, 100% RH/2 atm, 168 hrs
Liquid Thermal Shock	(Condition B) -55°C/125°C, 1000 cycles
Unbiased HAST	130°C/85%, RH/2 atm, 96 hrs

Thermal Performance θja (°C/W)

The thermal performance of each die in the package is influenced by other die in the package. Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation for specific applications should be performed.

Electrical Performance

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

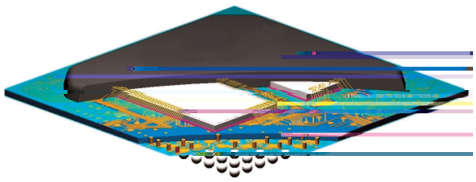
Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Inductance Mutual (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (2L)	2 - 7	34 - 119	1.3 - 4.55	0.26 - 2.28	0.25 - 0.95	0.06 - 0.42
Total (2L)		154 - 239	2.95 - 6.2	0.71 - 3.13	0.35 - 1.05	0.07 - 0.44
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (4L)	2 - 7	34 - 119	0.90 - 3.15	0.18 - 1.58	0.35 - 1.10	0.06 - 0.42
Total (4L)		154 - 239	2.55 - 4.80	0.63 - 2.43	0.45 - 1.20	0.07 - 0.44

Note: Net = Total Trace Length + Via + Solder Ball.

Cross Section

Package Size (mm)	Ball Count
15 x 15	74, 121, 160, 176, 196
17 x 17	208, 256
17.2 x 17.2	512
19 x 19	225, 233, 260, 324, 484
23 x 23	169, 192, 196, 208, 217, 225, 241, 304, 316, 324, 340, 360, 376, 388, 484
27 x 27	225, 256, 272, 292, 300, 316, 320, 324, 336, 352, 384, 388, 392, 400, 484, 484, 512, 625, 672
31 x 31	329, 353, 360, 385, 421, 433, 560, 604, 608, 676, 692, 701
35 x 35	312, 352, 363, 385, 388, 420, 452, 454, 456, 468, 492, 496, 512, 516, 544, 548, 564, 580, 680, 700, 740, 788
37.5 x 37.5	435, 625, 784, 840
40 x 40	503, 596, 600, 900, 928, 1253

Package Configurations



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